

S-Parameters Optimization in both Segmented and Unsegmented Insulated TSV upto 40GHz Frequency

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ABSTRACT

Segmented and unsegmented 3D insulated copper through silicon vias (TSVs) of diameter 10 micro-meter, height 100 micro-meter and silicon of sizes 100 micro-meter by 100 micro-meter by 100 micro-meter are modeled using analysis system (ANSYS), equivalent circuit using advanced design system (ADS) at frequency ranges between 100MHz and 40GHz and 10MHz step size. The segmented via is divided into three parts. Each part modeled separately. Scattering parameters are found. The outputs are optimized to give accurate results. The results show that the outputs reflect the transmission characteristics of an ideal TSV.

1 Introduction

S-Parameters Optimization in both Segmented and Unsegmented Insulated TSV was featured in [1]. This paper advances the work done in [1] by optimizing the S-Parameters but to a higher frequency of 40GHz. S parameters have been given much considerations since they allow a device to be treated as a black box with inputs and resulting outputs, making it possible to model a system without having to deal with the complex details of its actual structure.

However, the bandwidth of today's Integrated Circuits (IC's) keeps increasing. This paper has found it important to characterize their performance over wide frequency ranges up-to a maximum of 40GHz. This is because the traditional low-frequency parameters such as resistance, capacitance, and gain can be frequency dependent and therefore may not fully describe the performance of the IC at the desired frequency. Moreover, it may not be possible to characterize every parameter of a complex IC over frequency therefore system-level characterization using S-parameters may provide better and more reliable data [2, 3, 4].

In the previous paper [1], the scattering parameters especially the S₂₁ which defines power loss in TSVs was given much attention. Here we consider other parameters such as S₁₁ too.

2 S-Parameters

A simple RF relay is used to demonstrate the techniques of high-frequency model verification. It is considered a three-port device with an input, output and a control to switch the circuit on and off. However, since the device performance is independent of the control terminal it is simplified to a two-port device. Therefore, it is characterized by observing the behavior at its input and output terminals. This is elaborated in figure 1.

Where,

a_1 = incident wave on port 1

b_1 = reflected wave from port 1

a_2 = incident wave on port 2 (reflected from the load)

b_2 = reflected wave from port 2

Z_S = source impedance

Z_L = load impedance

From figure 2 notations, S-parameters defined the reflected waves b_1 and b_2 as shown in equation (1) and (2)

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (1)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (2)$$

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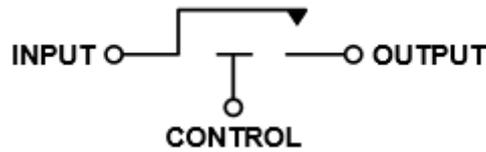


Figure 1: RF relay model [2]

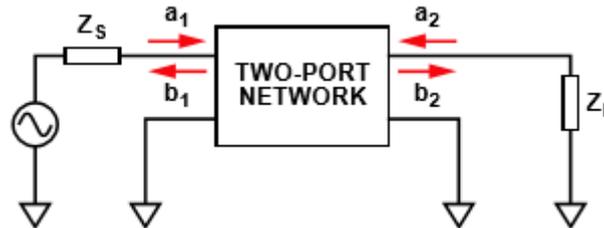


Figure 2: S-parameter model [2]

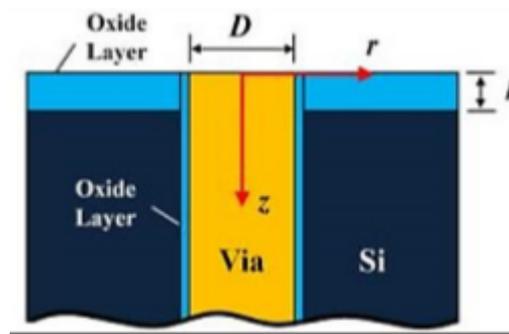


Figure 3: TSV structure [7]

If $Z_S = Z_0$, that is; impedance of two-port input, no reflections occur and $a_1 = 0$. If $Z_L = Z_0$ that is; the impedance of two-port output, no reflections occur and $a_2 = 0$. Therefore we can define the S-parameters, based on the matched condition as follows:

$$S_{11} = \frac{b_1}{a_1} \tag{3}$$

$$S_{22} = \frac{b_2}{a_2} \tag{4}$$

$$S_{21} = \frac{b_2}{a_1} \tag{5}$$

$$S_{12} = \frac{b_1}{a_2} \tag{6}$$

To realize the above parameters in a physical system, Z_S , Z_0 , and Z_L must be matched. For most systems this is easily implemented over a wide frequency range [2]. The authors implemented up to a maximum frequency of 40GHz.

3 Through Silicon Via (TSV) Technology

This study contributes to knowledge about parameter distribution, transmission properties, electrical effects and so on. This is the basic foundation of 3D IC [5, 6].

Figure 3 shows a structure of a TSV. It's made up of key areas such as via where the filler material is put. The filler material is copper in most cases since it's a good conductor. The letter z defines the via depth direction, D is the via diameter while r is the via radius direction. The TSV is surrounded by an oxide layer which is silicon dioxide and h defines its height or thickness. The whole model is done in silicon which is a substrate material. Increasing power, performance and financial bottle-necks beyond 3222 nm industry has led to development of TSV [8]. TSVs can be processed in different ways. For instance; Front

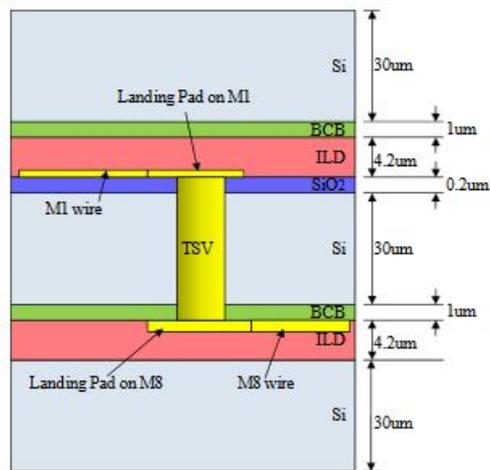


Figure 4: Via First TSV [9]

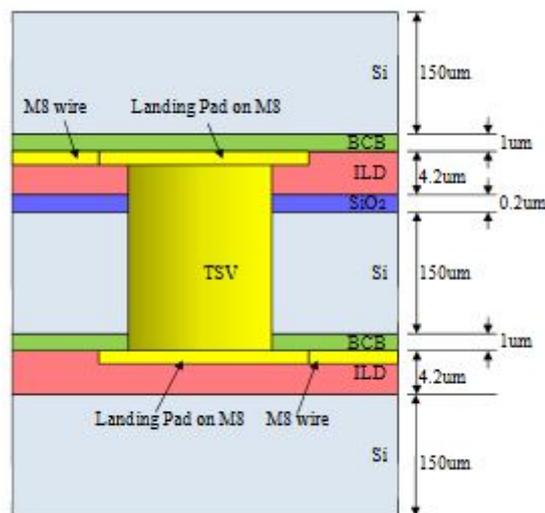


Figure 5: Via Last TSV [9]

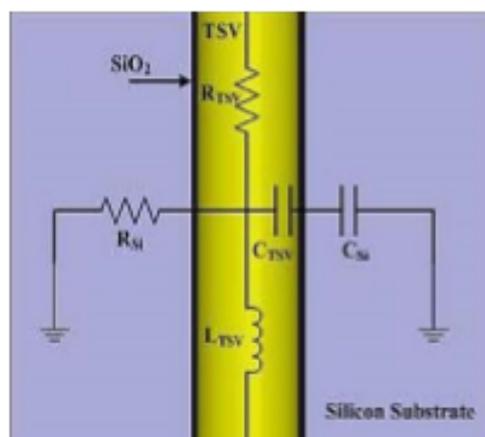


Figure 6: Unsegmented TSV model [6]

End Of Line (FEOL), Back End Of Line (BEOL), Via via) whereby TSVs are fabricated before the copper First (poly-silicon filled via) whereby TSVs are interconnects and Via Last (copper liner) where TSVs fabricated before transistors. Via Middle (copper filled are fabricated after bonding the stack. Figures 4 and

5 show the differences between via first and via last technologies. Potential reliability issues can arise due to during or after these processes. During the via design the stress management can be a problem. This is experienced through via fabrication which may induce tensile stresses in silicon, via may also experience compressive hoop stresses which could lead to via buckling, the quantity and spacing of via may also result in undesirable stress fields and finally the most common thermally induced stresses due to coefficient of Thermal Expansion (CTE) mismatch which may lead to cracking of the silicon wafer. Thermal management is another design problem. This is due to large and non-uniform heat flow within the package. There also exists redundancy in the design used.

Apart from the problems experienced during design of TSVs, some problems are experienced during processing. These include; metal voiding which happens during material filling, uniform via wall material deposition, active Integrated Circuit (IC) surface connectivity and wafer handling problem. Other challenges are experienced during the performance of the TSVs. For instance; limited reliability, thermal cycling, electro migration, silicon depletion at or around the via and also shock and vibration. Noise coupling, fabrication process limits and failure issues have been discussed in [10]. However TSV has several advantages such as reducing the delay, power and area. It also promotes the integration of heterogeneous devices.

4 TSV Liner

Although the TSV has several advantages, these would not be viable unless the TSV is well protected. This is enhanced by TSV liner. In our paper we propose the use of silicon dioxide material as a liner due to its many advantages. Dielectric liner functions as electrical isolation between the TSV metal fill and silicon substrate; therefore it should have zero leakage, high breakdown voltage, low stress, process temperature compatibility, good step coverage and uniformity. Silicon dioxide has these properties. However, other materials such as nitride and polymers are also used as liners for TSV applications [11,12, 13].

5 Methodology

There are several ways of characterizing the ports behavior. One is by admittance matrix Y or impedance matrix Z which defines the relationship between voltages and currents at the ports [14]. Various ways are available and are used to calculate functions that can accurately produce port characteristics within a desired frequency at the same time meet the physical requirements such as symmetry, causality, stability and passivity [15,16, 17 and 18]. The second way of characterizing the port behavior is by use of the incident and reflected waves that are related through the scattering parameter matrix [14], [19], [20]. This second

way is often applicable in high speed electronics modeling over the admittance formulation because it gives more accurate results at very high frequencies; it is also useful in applying pure transfer functions models in a simulation. These transfer function capability provides an easy way of observing internal voltages and currents in a subnetwork represented by a Y -, Z - or S -parameter-based port equivalent, and it reduces the computational burden of the model identification process as the number of ports is reduced [14].

As discussed in, [14], Y parameter models can be interfaced with electromagnetic transients program tools through equivalent circuits [21], [22]. However, the circuit experiences inaccuracy hence should be avoided and instead the model can be represented using convolutions [23], [24] which are considered a little bit standard as per [25, 26]. This paper is accessing the variation of S -parameters on a single insulated unsegmented TSV and segmented TSV over a frequency range of 40GHz. The S_{21} parameter which represents the insertion loss is the key area of research. Insertion loss is expected to be as low as possible on the graphs. The equivalent circuits of the unsegmented and segmented vias are simulated and the results represent the TSV characteristics. The segmented TSV gave a much lower insertion loss as compared to the unsegmented one. This shows that its more reliable and can be used to alleviate the insertion loss problem mainly experienced in the TSV thereby alleviating that reliability problem in 3D packages. The S parameters are converted to Z parameters, Z_{21} which gave much lower values than the S_{21} but still maintained the TSV characteristics. S_{11} characteristics are also listed.

5.1 Unsegmented TSV

Figure 6 represents a vertical TSV model. The R_{TSV} , C_{TSV} and L_{TSV} represent resistance, capacitance and inductance respectively along the TSV. R_{Si} and C_{Si} are the resistance and capacitance respectively in the silicon substrate.

The Advanced Design System (ADS) simulator developed the schematic in figure 7 from the model in figure 6. L_{TSV} , R_{TSV} and C_4 are inductance, resistance and capacitance respectively along the TSV. The C_1 and C_2 are capacitances in the TSV liner, R_{Si} and C_{Si} are the resistance and capacitance respectively along the silicon substrate, S parameter with the terms give the insertion and other losses experienced in TSV while the yield ensures accurate results are obtained. The schematic is an improvement of the work done in [1, 6]. In [6], silicon dioxide layer which act as a TSV liner was not included in the circuit. Moreover, optimization was not done to enhance accurate results. This has been done in this paper by including the yield in the system the frequency has been extended to 40GHz too. A total of 250 trials were made to finally end up with 100 percent yield. The trials were done within the frequency ranges specified in the S -parameter icon. S_{11} parameters have also been discussed.

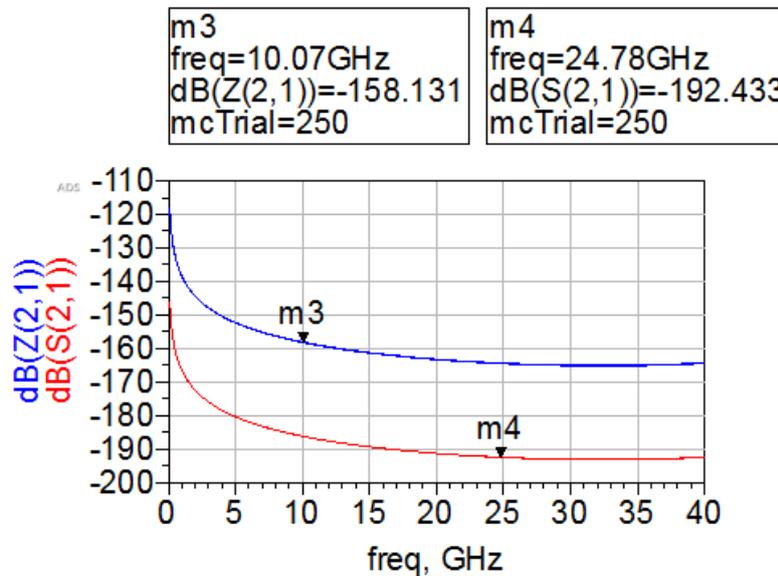


Figure 10: Unsegmented TSV graph

freq	S(1,1)	
	mcTrial=0	mcTrial=250
100.0 MHz	1.000 / 179.989	1.000 / 179.989
110.0 MHz	1.000 / 179.987	1.000 / 179.988
120.0 MHz	1.000 / 179.986	1.000 / 179.987
130.0 MHz	1.000 / 179.985	1.000 / 179.986
140.0 MHz	1.000 / 179.984	1.000 / 179.985
150.0 MHz	1.000 / 179.983	1.000 / 179.984
160.0 MHz	1.000 / 179.982	1.000 / 179.983
170.0 MHz	1.000 / 179.980	1.000 / 179.981
180.0 MHz	1.000 / 179.979	1.000 / 179.980
190.0 MHz	1.000 / 179.978	1.000 / 179.979
200.0 MHz	1.000 / 179.977	1.000 / 179.978
210.0 MHz	1.000 / 179.976	1.000 / 179.977
220.0 MHz	1.000 / 179.975	1.000 / 179.976
230.0 MHz	1.000 / 179.974	1.000 / 179.975
240.0 MHz	1.000 / 179.972	1.000 / 179.974
250.0 MHz	1.000 / 179.971	1.000 / 179.973
260.0 MHz	1.000 / 179.970	1.000 / 179.972
270.0 MHz	1.000 / 179.969	1.000 / 179.970
280.0 MHz	1.000 / 179.968	1.000 / 179.969
290.0 MHz	1.000 / 179.967	1.000 / 179.968
300.0 MHz	1.000 / 179.966	1.000 / 179.967
310.0 MHz	1.000 / 179.964	1.000 / 179.966

Figure 11: S11 list of values in unsegmented TSV

lator layer silicon dioxide. The LTSV, RTSV and C4 are the inductance, resistance and capacitance respectively along the TSV. RSi and CSi are the resistance and capacitance respectively along the silicon substrate. The S-parameter and the yield simulators play the same role as in figure 7.

6 Results and Discussions

6.1 Unsegmented TSV

Figure 10 looks exactly as what was done in [1] but the difference is that the frequency range has been stretched to 40GHz. The dB values are decreasing with the increased frequency. The markers, m3 and

m4 define the dB values at those particular frequencies.

Figure 11 is a list of S11 parameters with varying frequencies. As the frequency increases the S11 value decreased as evident in the list.

6.2 Segmented TSV

Figure 12 describes the dB(S(2,1)) with variation in frequency up to 40GHz. The m3 and m4 in this figure defined the parameter at those frequencies. However, the maximum power on the 'YIELD SPEC' was varied to enhance smooth curve; dB(Z(2,1)) was not plotted too, although the graph gave exactly the variations discussed in [1].

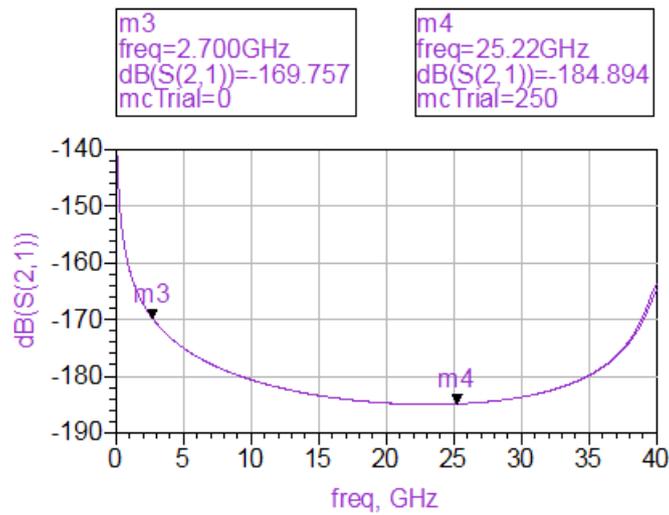


Figure 12: Segmented TSV graph

freq	S(1,1)	
	mcTrial=0	mcTrial=250
100.0 MHz	1.000 / 179.990	1.000 / 179.990
110.0 MHz	1.000 / 179.989	1.000 / 179.989
120.0 MHz	1.000 / 179.988	1.000 / 179.988
130.0 MHz	1.000 / 179.987	1.000 / 179.987
140.0 MHz	1.000 / 179.986	1.000 / 179.986
150.0 MHz	1.000 / 179.985	1.000 / 179.985
160.0 MHz	1.000 / 179.984	1.000 / 179.984
170.0 MHz	1.000 / 179.983	1.000 / 179.983
180.0 MHz	1.000 / 179.982	1.000 / 179.982
190.0 MHz	1.000 / 179.981	1.000 / 179.981
200.0 MHz	1.000 / 179.980	1.000 / 179.980
210.0 MHz	1.000 / 179.979	1.000 / 179.979
220.0 MHz	1.000 / 179.978	1.000 / 179.977
230.0 MHz	1.000 / 179.977	1.000 / 179.976
240.0 MHz	1.000 / 179.976	1.000 / 179.975
250.0 MHz	1.000 / 179.975	1.000 / 179.974
260.0 MHz	1.000 / 179.974	1.000 / 179.973
270.0 MHz	1.000 / 179.973	1.000 / 179.972
280.0 MHz	1.000 / 179.972	1.000 / 179.971
290.0 MHz	1.000 / 179.971	1.000 / 179.970
300.0 MHz	1.000 / 179.970	1.000 / 179.969
310.0 MHz	1.000 / 179.969	1.000 / 179.968
320.0 MHz	1.000 / 179.968	1.000 / 179.967
330.0 MHz	1.000 / 179.967	1.000 / 179.966
340.0 MHz	1.000 / 179.966	1.000 / 179.965
350.0 MHz	1.000 / 179.965	1.000 / 179.964

Figure 13: S11 list of values in Segmented TSV

Figure 13 on the other hand described S11 parameter with varying frequencies. It was noted that just like in the unsegmented TSV, the S11 values decreased with increased frequencies, the differences in S11 are however slight. However, The S11 in the segmented TSV is slightly higher than that in unsegmented one at the same frequency.

7 Conclusions and Recommendations

Both segmented and unsegmented TSV were modeled using ADS software. This work was an improvement of work done by [1 and 6]. In the previous work [1], the maximum frequency range considered

was 20GHz but in this paper, it has been stretched to 40GHz. We recommend extension of the frequency range because by doing so, its application will be possible on more electronic devices made. Optimization of the values also promotes more accurate results. Just like in the previous work we intend to do the modeling of TSV in more portions rather than three parts in future. We will also include the effects of changes in length and thickness of the TSV alongside use of other TSV liner materials such as polymers on the power losses. With more factors put into consideration, we hope to reduce the insertion losses in TSV even further. There has been increasing need of cheaper and high performance devices in the world today. These have made researches seek for solutions to these problems. Figure 14 describes the future of TSVs. Varia-

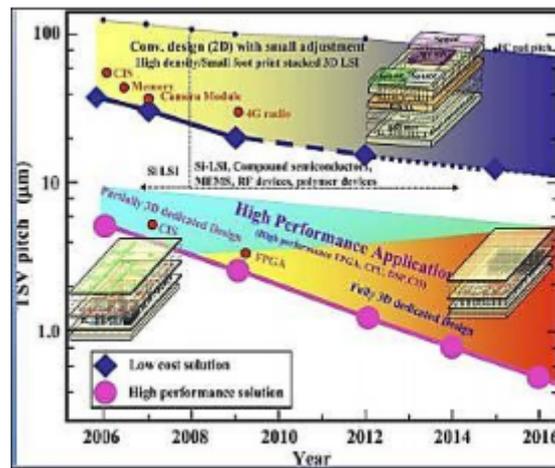


Figure 14: The future of TSV

tion of TSV pitch have greatly influenced the cost and performance of TSV which later influence the devices made between the year 2006 and the current 2017. In the year 2006, the cost of manufacturing TSVs was too high yet the performance of the devices made from the technology was poor due to high TSV pitch. This reduced the reliability of the electronic devices made [1].

Just like in [1], as years went by, research was done and the researchers realized that the TSV pitch size greatly influenced the cost and performance of the TSV modeled devices. They therefore proposed the reduction of the TSV pitch from 100 micro-meters in the year 2006 to less than 1 micro-meter now; 2017. Through the gradual reduction in the TSV pitch size, the cost of production has gone down and the performance of the electronic devices made from the TSV technology has increased. High costs and low performance was evident in 2D conventional designs. However, the use of semiconductors, MEMS, RF devices and polymer devices enhanced development of partially 3D dedicated design to fully 3D dedicated designs which experience low costs and high performance.

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