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Optimal Synthesis of Universal Space Vector Digital Algorithm for Matrix Converters

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ABSTRACT

This paper presents the synthesis of a dynamic space vector modulation for power matrix converters so that it is possible to implement a universal modulator that provides a control algorithm dynamically optimized according to the requirements for the matrix converter.

1. Introduction

In recent years the three-phase to three-phase matrix converter has received considerable attention as an alternative to hard and soft switching dc link converters. This paper is an extension of work originally presented in International Symposium on Electronics and Telecommunications ISETC '16 Twelfth Edition [1]. The SVM (space vector modulation) control strategy for matrix converter offers the best performance, maximal voltage gain and controllable input displacement factor. There are several possible SVM algorithms focused first on reducing energy losses or optimizing the parameters for output voltage and input current [2]. The optimum choice of one of the SVM techniques is a complex task because these requirements are contradictory since reduced power losses mean a reduced sampling frequency leading to a degree of large distortion of waveforms generated by the matrix converter. So for choose correctly a control technique it is required a prior accurate knowledge of the specific conditions which the matrix converter will operate and the characteristics of semiconductor devices which implement the bidirectional switches [3]. Therefore, depending by the operation mode of the power circuit and the conditions imposed by the nature of the load it is useful an implementation of an universal algorithm enabling the transition from an reducing energy losses mode to a very low distortion of the generated waveforms mode and possibility to operation intermediate regimes between them. For this reason it is necessary to implement a digital modulator circuit that allows switching from one SVM algorithm to another without major modifications of the hardware control circuit.

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2. Space Vector Modulation

The matrix converter consists of nine bidirectional switches that connect the three outputs with each of the three inputs, as shown in Figure 1. The converter being supplied by a voltage source, the three input phases can't be short-circuited, and the load having generally a mainly inductive character, the load current can't be interrupted. Because of these constraints the nine switches can generate only 27 permitted combinations. The SVM control algorithm uses 21 of these combinations, a number of 18 combinations, A122- A133; B212-B313 and C221-C331 which connect two output phases at the same input, called active states and a number of 3 combinations Z111-Z333 with all three outputs connected at the same input, called passive states of the matrix converter. To analyze the SVM modulation applied to a three-phase system x1, x2, x3, the space vector X of the system can be used, represented in the complex plan according to the transformation:

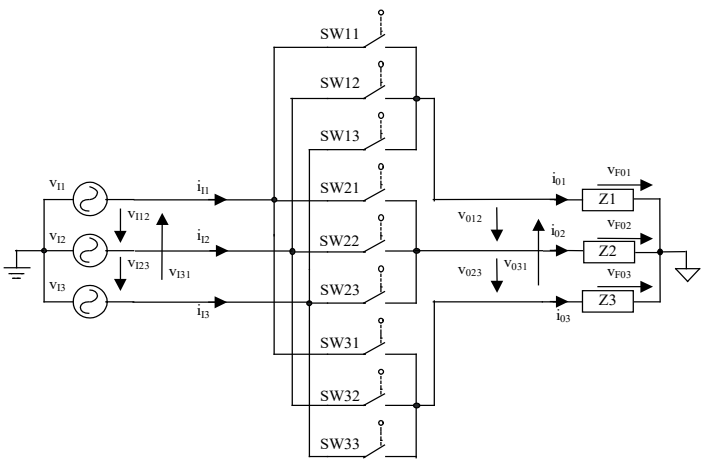

Figure 1: The matrix converter switch layout

$$\underline{X} = Re(\underline{X}) + j\, IM(\underline{X}) = 2/3\,(x_1 + \underline{a}\,x_2 + \underline{a}^2 x_3) \quad (1)$$

where $\underline{a} = e^{j\,2\pi/3}$.

According to this transformation the desired output line voltages space vector is $\underline{V}_{0LW}$ which rotates with the ω_0 angular speed, and the desired input phase currents space vector is $\underline{I}_{IW}$ which rotates with ω_I angular speed as shown in Figure 2 and Figure 3 respectively.

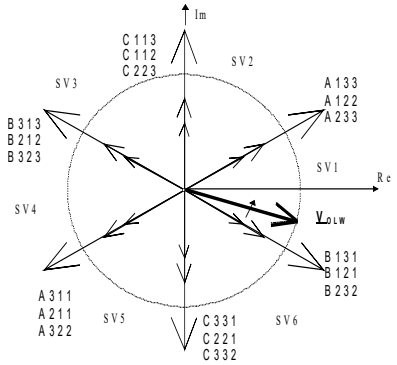

Figure 2: Output voltage SVM vectors diagram

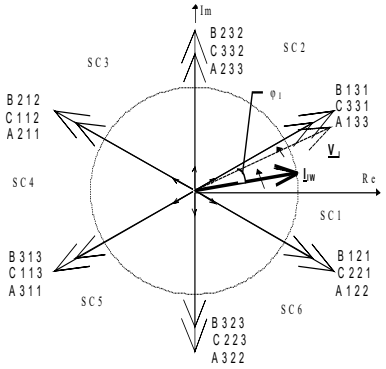

Figure 3: Input current SVM vectors diagram

The circular trajectories of these vectors can be divided in six voltage and current sectors, *SV* and *SC* respectively. If *Ts* time interval is short enough so that the reference vectors $\underline{V}_{OLW}$ and $\underline{I}_{IW}$ do not change significantly, the mean vector space result from different combinations of stationary space vector and null corresponding input voltage line will be equal with the reference vector in this time. Simultaneously it must be performed the desired phase difference between the input current reference space vector and the input voltage space vector, through various combinations of stationary and null space vector corresponding to input currents. The best approximation of spatial reference vector at a time, can be done using vectors that have direction adjacent with the reference space vector [2]. The principle is shown in Figure 4a and Figure 4b, where *a,b* and *m,n* are adjacent directions for output voltage reference space vector and input current reference space vector, respectively. In Figure 4c and Figure 4d it is shown how to choose the vectors for SV1 and SC1 active sectors. In this way from the 21 matrix converter permitted states, in any moment only four active states uniquely established and one of the passive states can simultaneously synthesise the two reference vectors [4]. The order of these active states and the passive state required in a sampling period are chosen so that the number of switches is minimum. Using the trigonometric laws, the normalised time intervals in a sampling period *Ts*, corresponding to the four active states can be established:

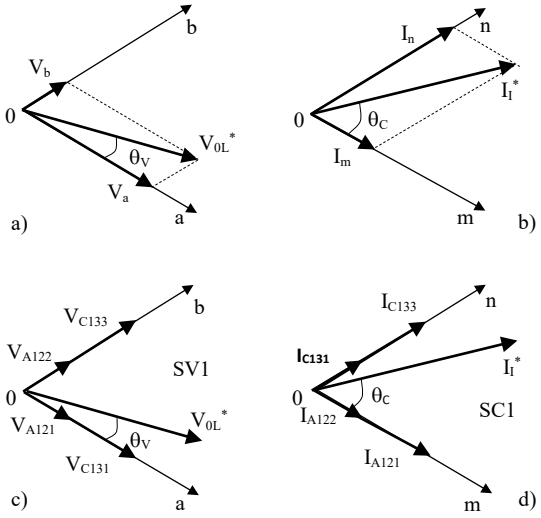

Figure 4: The space vector modulation principle

$$h_{am} = \frac{2}{\sqrt{3}} * (\frac{V_{OL}}{V_{IL}}) * \frac{\sin(\pi/3 - \theta_V) * \sin(\pi/3 - \theta_C)}{\cos(\varphi_I)} \quad (2)$$

$$h_{an} = \frac{2}{\sqrt{3}} * (\frac{V_{OL}}{V_{IL}}) * \frac{\sin(\pi/3 - \theta_V) * \sin(\theta_C)}{\cos(\varphi_I)} \quad (3)$$

$$h_{bm} = \frac{2}{\sqrt{3}} * (\frac{V_{OL}}{V_{IL}}) * \frac{\sin(\theta_V) * \sin(\pi/3 - \theta_C)}{\cos(\varphi_I)} \quad (4)$$

$$h_{bn} = \frac{2}{\sqrt{3}} * (\frac{V_{OL}}{V_{IL}}) * \frac{\sin(\theta_V) * \sin(\theta_C)}{\cos(\varphi_I)} \quad (5)$$

where $h_{am}=T_{am}/T_S$, $h_{an}=T_{an}/T_S$, $h_{bm}=T_{bm}/T_S$, $h_{bn}=T_{bn}/T_S$ an and $1-h_{am}-h_{an}-h_{bm}-h_{bn}=h_z$ [2].

For example, the relation between output and input voltages is

$$\left[v_0^*\right]=\begin{bmatrix} v_{01}^* \\ v_{02}^* \\ v_{03}^* \end{bmatrix}=\begin{bmatrix} 1 & 0 & 0 \\ h_z & h_{am}+h_{bm} & h_{an}+h_{bn} \\ h_{am}+h_{an}+h_z & h_{bm} & h_{bn} \end{bmatrix}\cdot\begin{bmatrix} v_{11} \\ v_{12} \\ v_{13} \end{bmatrix} \quad (6)$$

for *SV1* and *SC1* active sectors. This fact means that the normalised time intervals h_{am}, h_{an}, h_{bm}, h_{bn}, h_z represent the transfer functions for the SVM control strategy.

3. SVM1-SVM3 Versions of Space Vector Modulation

For a three-phase voltage supply for a given three phase output voltages and input phase shift between current and voltage, the association between active SVM and permitted matrix converter states is unique (Table 1). If you know the T_S, then periods T_{am}, T_{bm}, T_{an}, T_{bn}, can be calculated with relationships (2)-(5). In the time interval T_z the matrix converter can pass in any of the passive states. The order in which matrix converter switches from one state to another, within the time T_S, does not affect the local average value of voltages and currents [2],[5]. Basically, choosing between passive states and the order in which the converter switches from one state to another, does not affect the fundamental components of generated waveforms, but it determines the number of commutations required per unit time and the spectral characteristics of generated waveforms. Generally it is intended that the arrangement of the matrix converter states matrix in a sampling period T_S is made such that are necessary as few commutations when passing from one state to another. For example if the active sectors are *SV1* and *SC1* respectively, then from Table 1, the correlation between active states and switching states is *am, bm, an, bn* and *A121, A122, C131, C133* respectively. If a sampling period will use the SVM sequence *am - bm - bn - an -z* , then this corresponds to sequence *A121 -(1)- A122 -(1)- C133 -(2)- C131 -(1)- Z111-(1)-...*, if the z state is associated with Z111state. It is noted that in this case 6 switching are required within the sampling period T_S. If it is kept the same SVM sequence and combination of active sectors is SV1-SC2 then the sequence becomes *C131 -(1)- C133 -(1)- B233 -(1)- B232 -(3)- Z111-(1)-...* which means that required 7switching/T_S. But if the SVM combination is changed as follows *bm - am - an - bn -z* , then we have the next switching sequence: *C133 -(1)- C131 -(2)- B232 -(1)- B233 -(1)- Z333-(1)-...*, if zero state is associated with *Z333* state. It is noted that in this case it is required 6switching/T_S too. Generalizing for all possible combinations it is obtained the Table 2 association which can be easily implemented in a digital control system. Depending on the combination of the active sectors at a time, we define the complementary logical variables *Pa* and *Pb*, as follows:

$$Pa=(SV1+SV3+SV5)(SC1+SC3+SC5)+(SV2+SV4+SV6)(SC2+SC4+SC6) \quad (7)$$

$$Pb=(SV1+SV3+SV5)(SC2+SC4+SC6)+(SV2+SV4+SV6)(SC1+SC3+SC5) \quad (8)$$

Table 1: Matrix converter active states and SV,SC sectors association

Voltage Sector SV	Current Sector SC	Active State am	Active State bm	Active State an	Active State bn
1	1	A121	A122	C131	C133
1	2	C131	C133	B232	B233
1	3	B232	B233	A212	A211
1	4	A212	A211	C313	C311
1	5	C313	C311	B323	B322
1	6	B323	B322	A121	A122
2	1	A122	A112	C133	C113
2	2	C133	C113	B233	B223
2	3	B233	B223	A211	A221
2	4	A211	A221	C311	C331
2	5	C311	C331	B322	B332
2	6	B322	B332	A122	A112
3	1	A112	A212	C113	C313
3	2	C113	C313	B223	B323
3	3	B223	B323	A221	A121
3	4	A221	A121	C331	C131
3	5	C331	C131	B332	B232
3	6	B332	B232	A112	A212
4	1	A212	A211	C313	C311
4	2	C313	C311	B323	B322
4	3	B323	B322	A121	A122
4	4	A121	A122	C131	C133
4	5	C131	C133	B232	B233
4	6	B232	B233	A212	A211
5	1	A211	A221	C311	C331
5	2	C311	C331	B322	B332
5	3	B322	B332	A122	A112
5	4	A122	A112	C133	C113
5	5	C133	C113	B233	B223
5	6	B233	B223	A211	A221
6	1	A221	A121	C331	C131
6	2	C331	C131	B332	B232
6	3	B332	B232	A112	A212
6	4	A112	A212	C113	C313
6	5	C113	C313	B223	B323
6	6	B223	B323	A221	A121

Table2: Sequence SVM states and voltage current sectors association for 6switchings/T_S

Active Sectors	SVM States Sequence
SV1-SC1 SV1-SC3 SV1-SC5 SV2-SC2 SV2-SC4 SV2-SC6 SV3-SC1 SV3-SC3 SV3-SC5 SV4-SC2 SV4-SC4 SV4-SC6 SV5-SC1 SV5-SC3 SV5-SC5 SV6-SC2 SV6-SC4 SV6-SC6	*am - bm - bn - an -z*
SV1-SC2 SV1-SC4 SV1-SC6 SV2-SC1 SV2-SC3 SV2-SC5 SV3-SC2 SV3-SC4 SV3-SC6 SV4-SC1 SV4-SC3 SV4-SC5 SV5-SC2 SV5-SC4 SV5-SC6 SV6-SC1 SV6-SC3 SV6-SC5	*bm - am - an - bn -z*

This SVM version can be changed if the passive state *z* is placed at the beginning of the sampling period *z- am- bm- bn -an* for *Pa =1* and *z- bm- am- an- bn* for *Pa =0* or *z- an- bn- bm- am* and *z- bn- an- am- bm* for *Pa=1* and *Pa=0*, respectively. The combination of the SVM sequences and the matrix converter states can be easily implemented by some memory circuits. The variant thus obtained will be referred to as SVM1. This principle

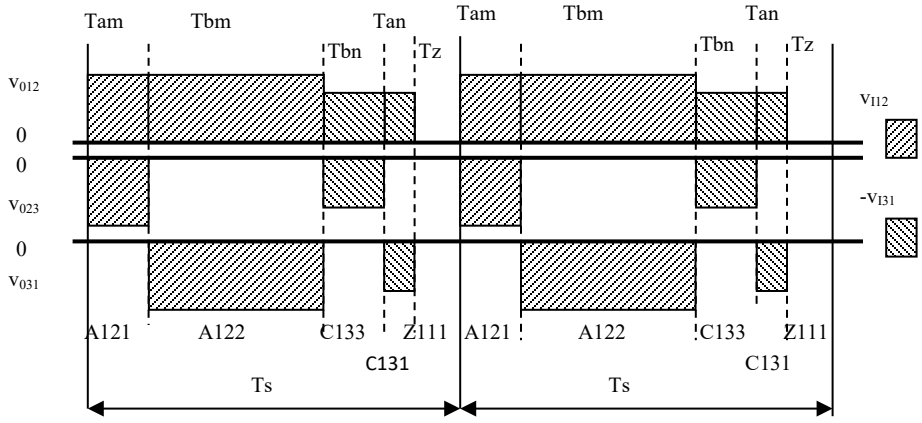

Figure 5: Line output voltage generation in the sampling period for SVM1 algorithm

is shown in Figure 5 for a sampling period. Again 6 switchings/T_S are necessary if for *Pa =1* the SVM sequence is *an- bn- bm- am - z* and for *Pa =0* it is *bn- an- am- bm- z* . Tis s SVM1a algorithm. The SVM1 version can be modified if the zero state is at the beginning of the sequence *z- am – bm –bn – an* for Pa=1 and *z- bm – am – an - bn*. for Pa=0. This is SVM1b algorithm.

By modifying the SVM1 algorithm in the same way we can get the algorithm SVM1c ie *z- an – bn –bm – am* for Pa=1 and *z- bn – an – am - bm*. for Pa=0. Again 6 switchings/T_S are necessary if the passive state is placed between active states*: bm- am- z- an- bn* and *am- bm- z- bn- an* for *Pa =1* and *Pa =0* or *bn- an- z- am- bm* and *an- bn- z- bm- am* for *Pa =1* and *Pa =0* synthesizing another algorithms named SVM1d and SVM1e respectively. A further reduction in the number of commutations can be made by combining certain type of previous algorithms. These new combinations will be named SVM2. A first additional reduction in the number of commutations can be done if for three consecutive sampling periods the SVM sequences will be *SVM1b - SVM1e - SVM1* or *SVM1c - SVM1d - SVM1a*, versions thus obtained are called SVM2a and SVM2b. For example, for SVM2a and *SC1-SV1* active sectors the SVM sequence will be *z- am- bm- bn- an- bn- an- z- am-bm- am- bm- bn- an- z* for *Pa =1*, which means that the number of commutation will be reduced with 5.5%. It can also be reduced the number of switching whether to combine two types of SVM1 sequences for two consecutive sampling periods in sequences *SVM1-SVM1c, SVM1a-SVM1b* and *SVM1d-SVM1e,* synthesizing the control techniques SVM2c, SVM2d and SVM2e, respectively. For example for SVM2c and SV1-SC1 active sectors, if Pa =1 the matrix converter sates will be *A121-(1)-A122-(2)-C133-(1)-C131-(1)-Z111-(0)-Z111-(1)-C131-(1)-C133 -(2)-A122-(1)-A121-(0)-* therefore it means that two consecutive sampling periods requires 10 switching so that the average switching requires 5switchings/T_S. This means a 16% reduction in the necessary number of commutations.

Another direction is optimization techniques to control the dominant harmonics, movement of these to high frequencies, for the same sampling frequency, without increasing excessive the switching losses. This can be achieving using symmetrical waveforms to the center of the sampling period [3]. Variants proposed in the literature accomplishes this balancing around the passive state, which is placed in the center of the sampling period, being framed by the active states that are divided into equal time intervals placed at the beginning and the end of the sampling period. To minimize the number of necessary switching sequences the implementation of SVM sequences proposed in this paper are *am/2- bm/2- bn/2- an/2- z- an/2- bn/2- bm/2- am/2* for *Pa =0* and *bm/2- am/2- an/2- bn/2- z- bn/2- an/2- am/2- bm/2* for *Pa=1*. This version is named SVM3. For this type of algorithms, the converter switches between 9 states during a sampling period, so the minimum number of commutations required is 8switching/T_S. If the SVM sequences are *an/2- bn/2- bm/2- am/2- z- am/2- bm/2- bn/2- an/2* for *Pa =0* and *bn/2- an/2- am/2- bm/2- z- bm/2- am/2- an/2- bn/2 for Pa =1* then are necessary 8switching/TS too. This is named SVM3a algorithm. For SVM3 the output voltage is symmetrical around "big" pulses, while for SVM3a it is symmetrical around "low" pulses for angle θ_C=0-30° in each current sector and vice versa for θ_C =30-60°. În [4] it is suggested that maintaining symmetry around the “big” or “small” voltage pulses regardless of the angle θ_C this can improve the quality of spectral waveforms generated at the converter output matrix. If for θ_C =0-30° will be used SVM3a and for θ_C =30-60° will be used SVM3, then at any time the output voltage waveform will have a shape symmetrical around “small” voltage pulses. This is SVM3b technique. If it is used SVM3 for θ_C =0-30° and SVM3a for θ_C =30-60°we will have symmetry around „large” pulses. This is SVM3c. An improvement of the quality of the frequency spectrum for the waveforms generated by the matrix converter can be obtained by alternating "big" voltage pulses with "small" voltage pulses keeping the symmetry of the output voltages [4]. In order to implement this technique it is necessary to control all switchings between nine states that requires 10 switching/T_S which results in an increase of 66% in the number of switching per unit time. To implement this technique it is necessary to control all switching between nine states. But if in a sampling period is chosen the sequence *bn/2- an/2- z/2- am/2- bm- am/2- z/2- an/2- bn/2* for *Pa =1* and *an/2- bn/2- z/2- bm/2- am- bm/2- z/2- bn/2- an/2* for *Pa =0* or *bm/2- am/2- z/2- an/2- bn- an/2- z/2- am/2- bm/2* and *am/2- bm/2- z/2- bn/2- an- bn/2- z/2- bm/2- am/2*, for *Pa =1* and *Pa =0* respectively then it is possible to reduce the

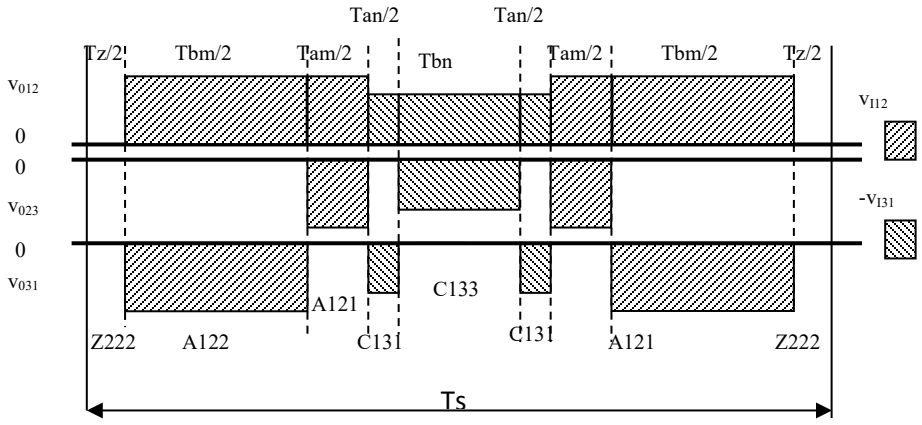

Figure 6: Line output voltage generation in the sampling period for SVM3d algorithm

number of commutation to 8commutations/T_S. This is SVM3d algorithm. If the sequences are *z/2-bn/2- an/2- am/2- bm- am/2- an/2- bn/2- z/2* for Pa=1 and *z/2-an/2- bn/2- bm/2- am- bm/2- bn/2- an/2- z/2* for Pa=0 then we obtain version SVM3e. For angle θ_C=0-30°, SVM3d generates symmetrical waveforms around the „small" voltage pulses like in Figure 6 and SVM3e around "big" voltage pulses, and θ_C =30-60° we have a reversed situation. If for θ_C=0-30° we will use SVM3e and for θ_C =30-60° we will use SVM3d, then at any time the output voltage waveform will be symmetrical around "high" pulses and the algorithm will be named SVM3f. If for θ_C=0-30° we will use SVM3d and for θ_C =30-60° we will use SVM3e, then at any time the output voltage waveform will be symmetrical around "small" pulses and the algorithm will be named SVM3g. If in a sampling period it is chosen the sequence *bn/2- an/2- z/2- am/2- bm- am/2- z/2- an/2- bn/2* for Pa =1 and *an/2- bn/2- z/2- bm/2- am- bm/2- z/2- bn/2- an/2* for Pa =0 we will obtain SVM3h. If for Pa =1 and Pa =0 we will have *bm/2- am/2- z/2- an/2- bn- an/2- z/2- am/2- bm/2* and *am/2- bm/2- z/2- bn/2- an- bn/2- z/2- bm/2- am/2* respectively then we will obtain SVM3i. These algorithms are characterized by 8 switchings/T_S too, the waveforms being symmetrically around the center of tha sampling period. The output voltages consist of alternative "high" and "small" voltage pulses set apart by intervals of "zero" voltage. Combining SVM3i and SVM3h in the same manner we will be obtain SVM3i and SVM3k characterized by waveform that are symmetrical around only the "high" pulses or only around the "small" voltage pulses. A detailed analyses of these algorithms will be presented in a future paper.

4. Implementation of the SVM1-SVM3 Modulator

Whichever you choose to control SVM algorithm, a computer system will determine the value of transfer functions h_{am}, h_{an}, h_{bm}, h_{bn} şi h_z, at T_S time intervals. These transfer functions are then transformed into *S11-S33* switching functions, which controls the ON/OFF states of the 9 bidirectional switches. To convert these transfer functions in PWM switching functions are sufficient four timers TM1-TM4. For this calculus it is necessary to know the modulation index $m=V_{0L}/V_{0L\,max}$ *or* $V_0/V_{0\,max}$, space vector angles θ_C şi θ_V and input phase angle. Analyzing the proposed variants of SVM algorithm previous proposed it is noted that according to the sequence of matrix converter switching states are 12 possible combinations of timer intervals TM1-TM4, according to the timeframes $T_{am}=h_{am}\cdot T_S$, $T_{bm}= h_{bm}\cdot T_S$, $T_{an}= h_{an}\cdot T_S$, $T_{bn}= h_{bn}\cdot T_S$ and $T_z=h_z\cdot T_S$. These combinations, denoted *CTV1-CTV12* are presented in Table 3. For example for *CTV1* combination the logical signals *ST1-ST4* at the outputs of timers will be like in Figure7. The switching functions *S11-S33* associated with switches of the matrix converter are calculated based on the combinations of *CTV, SV, SC* variables and auxiliary variables *Pam, Pbm, Pbn, Pan and Pz* calculated based on the five possible states of the signals *ST1-ST4*. For example switching function formula for *S11* is given by equation (9).

$$S11 = Pam\ ((SC1+SC2)(SV1+SV2+SV3)+(SC4+SC5)(SV4+SV5+SV6))+Pbm\ ((SC1+SC2)(SV1+SV2+SV6)+(SC4+SC5)(SV3+SV4+SV5))+Pbn\ ((SC1+SC6)(SV1+SV2+SV6)+(SC3+SC4)(SV3+SV4+SV5))+Pan\ ((SC1+SC6)(SV1+SV2+SV3)+(SC3+SC4)(SV4+SV5+SV6))+Pz\ (Saz1\cdot(SC1+SC4)+Saz2\cdot(SC3+SC6)+Saz3\cdot(SC2+SC5)) \quad (9)$$

Formula (10) is an example calculation for auxiliary variable *Pam*

$$Pam = ST1\cdot ST2\cdot ST3\cdot ST4\cdot(CTV2\cdot CTV9)+\overline{ST1}\cdot ST2\cdot ST3\cdot ST4\cdot(CTV1\cdot CTV6\cdot CTV10)+\overline{ST1}\cdot\overline{ST2}\cdot ST3\cdot ST4\cdot(CTV3\cdot CTV5)+\overline{ST1}\cdot\overline{ST2}\cdot\overline{ST3}\cdot ST4\cdot(CTV4\cdot CTV7\cdot CTV12)+\overline{ST1}\cdot\overline{ST2}\cdot\overline{ST3}\cdot\overline{ST4}\cdot(CTV8\cdot CTV11) \quad (10)$$

Saz1-Saz3 variables are associated with the passive states *z* of the converter.

Table 3: The time intervals generated by timers

	TM1	TM2	TM3	TM4
CTV1	T_{bm}	$T_{bm}+T_{am}$	$T_{bm}+T_{am}+T_{an}$	$T_{bm}+T_{am}+T_{an}+T_{bn}$
CTV2	T_{am}	$T_{am}+T_{bm}$	$T_{am}+T_{bm}+T_{bn}$	$T_{am}+T_{bm}+T_{bn}+T_{an}$
CTV3	T_{bn}	$T_{bn}+T_{an}$	$T_{bn}+T_{an}+T_{am}$	$T_{bn}+T_{an}+T_{am}+T_{bm}$
CTV4	T_{an}	$T_{an}+T_{bn}$	$T_{an}+T_{bn}+T_{bm}$	$T_{an}+T_{bn}+T_{bm}+T_{am}$
CTV5	T_z	T_z+T_{bm}	$T_z+T_{bm}+T_{am}$	$T_z+T_{bm}+T_{am}+T_{an}$
CTV6	T_z	T_z+T_{am}	$T_z+T_{am}+T_{bm}$	$T_z+T_{am}+T_{bm}+T_{bn}$
CTV7	T_z	T_z+T_{bn}	$T_z+T_{bn}+T_{an}$	$T_z+T_{bn}+T_{an}+T_{am}$
CTV8	T_z	T_z+T_{an}	$T_z+T_{an}+T_{bn}$	$T_z+T_{an}+T_{bn}+T_{bm}$
CTV9	T_{am}	$T_{am}+T_{bm}$	$T_{am}+T_{bm}+T_z$	$T_{am}+T_{bm}+T_z+T_{bn}$

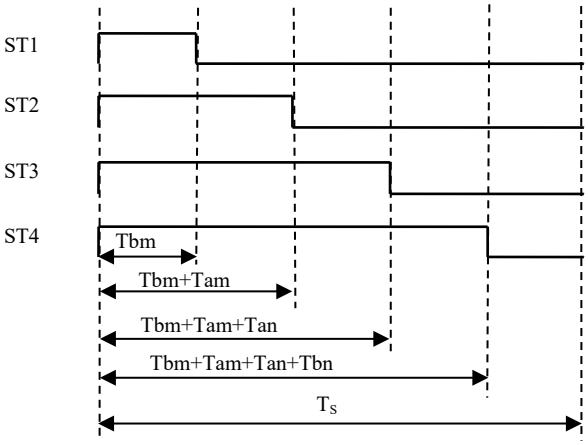

Figure 7: The logical signals at the timers output

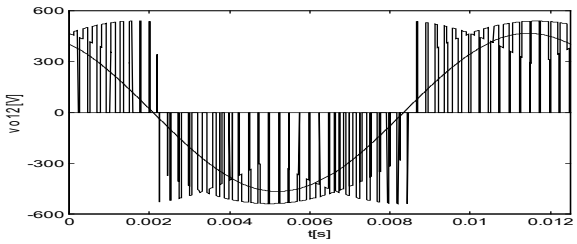

Figure: 8. Output line voltage waveform for SVM1 algorithm

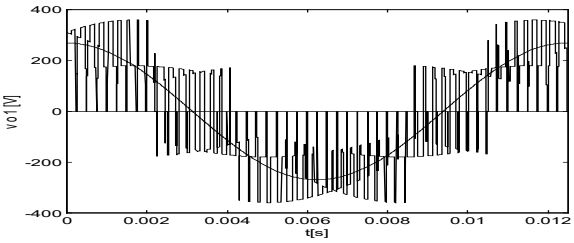

Figure 9: Output phase voltage waveform for SVM1 algorithm

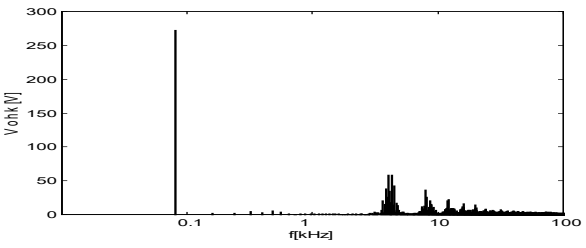

Figure 10: Frequency spectrum of phase output voltage for SVM1

CTV10	T_{bm}	$T_{bm}+T_{am}$	$T_{bm}+T_{am}+T_z$	$T_{bm}+T_{am}+T_z+T_{an}$
CTV11	T_{an}	$T_{an}+T_{bn}$	$T_{an}+T_{bn}+T_z$	$T_{an}+T_{bn}+T_z+T_{bm}$
CTV12	T_{bn}	$T_{bn}+T_{an}$	$T_{bn}+T_{an}+T_z$	$T_{bn}+T_{an}+T_z+T_{am}$

The output voltage waveforms and the frequency spectrum for SVM1 algorithm using S11-S33 switching functions generated with the universal modulator are presented in Figure 8, Figure 9 and Figure 10.

5. Conclusion

In this paper it was presented a dynamic algorithm that enables the implementation of a universal SVM1-SVM3 modulator to control the matrix converters. In this way it is possible to choose different control options that are optimized for reducing energy losses or to control the dominant harmonics. A more detail comparative analysis of these algorithms will be presented in a future work.

Conflict of Interest

The authors declare no conflict of interest.

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