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Applications of TCAD Simulation Software for Fabrication and study of Process Variation Effects on Threshold Voltage in 180nm Floating-Gate Device

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ABSTRACT

In this work, a study of the process variation effects on the threshold voltage of a floating-gate device is proposed. The study demonstrates the sensitivity of the threshold voltage to five geometrical parameters including gate length, gate width, tunneling gate oxide thickness, bottom oxide-nitride-oxide oxide thickness, and nitride spacer thickness. This paper also proposed a detailed flow to fabricate the floating-gate device for CMOS 180nm process, which is used to design the floating-gate device for the study. This paper used the TCAD tools including Athena, Devedit3D, and Atlas for the simulations.

1 Introduction

The CMOS technology has been developing over the past many years thanks to its benefits like high integration density, low fabrication costs, and high operating speeds. In addition, many novel techniques of circuit design have been shown ranging from memories, analog mixed-signal, RFIC [1] -[7] to mm-Wave IC design [8], [9].

Meanwhile, there has been considerable development in the semiconductor memory field. This field is divided into two main branches which are volatile memories and non-volatile memories, and these types of memories are developing based on the CMOS technology [10], [11]. While the former lose data when the power supply is off, the latter can retain the stored information even after power is removed. Therefore, non-volatile memories are used in a very wide variety of products like cell phones, computers, and communication [12]. Thus, many researchers have focused on the study of this kind of memory. However, to study the memories, the floating gate device needs to be investigated first since it is the core of the memories [13] –[15].

Focusing on designing a simulation model for the floating gate device, many parameters are studied under the process variation. There are two main methods to investigate the process variation effects. The first way is using the SPICE model. This is basically a fast method but the approach of this method lacks many conditions in the fabrication process like doping channel [16]. Therefore, the effects of the doping channel would not be studied. The other method is using the 3D-TCAD simulation for analyzing the geometrical parameters and the doping channel effects [17] -[19].

In this work, a detailed design flow and parameter values to fabricate the complete floating-gate device are proposed to investigate the structure and characteristics of the device. The process variation effects on the threshold voltage, which is a vital parameter of the device, are studied by using the TCAD simulation tools. Authors introduced the floating-gate device and presented ideas about how to study the process variation on threshold voltage in 180nm

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floating-gate device in the ”2019 19th International Symposium on Communications and Information Technologies (ISCIT)” [1] and the following paper is an extension of this work.

The remainder of this paper is organized as follows: Section II introduces an overview structure of the device in fabrication and the operation states also. Following this, the detailed flow and parameter values to fabricate a complete device are shown in section III. Next, section IV shows the analysis and discussion of the process variation results in the threshold voltage. This section also describes the simulation of operation states after fabricating. Finally, section V shows the conclusion.

2 Floating Gate Device

The floating-gate device is the core of almost modern non-volatile memories [20], [21]. With regards to fabrication, the device is recognized through the use of a ”floating gate”. The gate is completely surrounded by dielectrics [22]. A cross section of a device is given in Figure. 1. Being electrically isolated, the floating gate acts as the storing layer in the device. Therefore, the operation states of the device would be determined based on the status of the gate. More importantly, the insulator around the floating gate must be thick enough to prevent leakage of charges from the floating gate to the substrate when the power is off, and it also must be thin enough to allow the transfer of charges on and off the gate under appropriate bias configuration. Moreover, reducing the thickness of the insulator, especially the tunneling gate oxide thickness has been investigated to reduce the program/erase voltage and enhance the level of integration [13],[23].

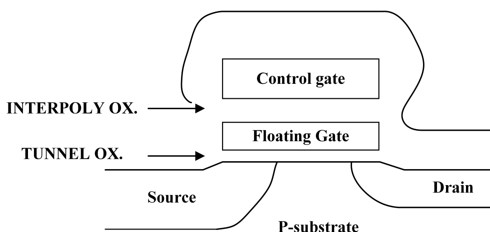

Figure 1: Floating-gate device structure in fabrication

The floating-gate device has three operation states which are programming, erasing, and reading. Programming refers to putting electrons called Channel Hot Electrons on the floating gate. In contrast, removing the electrons from the gate to the substrate would be performed in the erasing process. The removing current is renowned for the Fowler-Nordheim Tunnel current. Reading is used to determine if the device is programmed or erased.

3 Floating Gate Fabrication & Simulation

This flow proposes using an additional Epitaxial grow layer which was not used in traditional CMOS processes. The growth of an epitaxial layer over the P-type substrate offers some advantages including improving the performance of this device as well as floating-gate integrated circuits, minimizing latch-up effects that a CMOS circuit may undergo when powered up, and helping control the doping concentration of this device accurately [24].

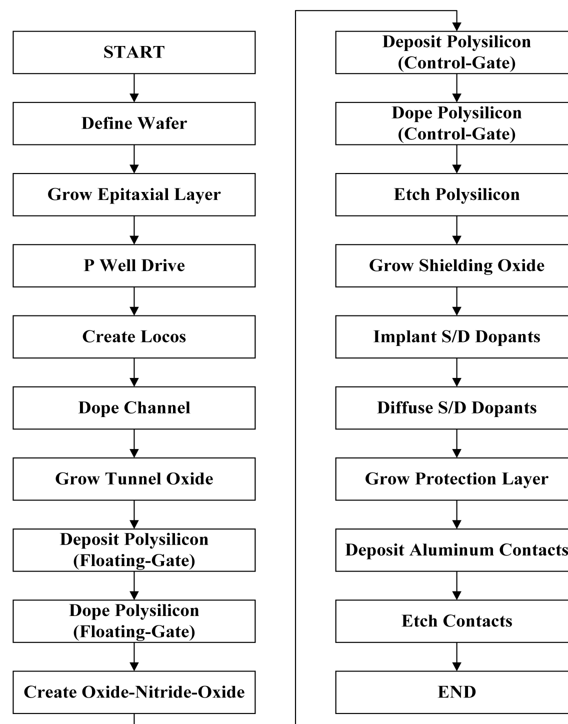

Figure 2: Floating-gate device design flow chart

The main difference in terms of structure between the floating-gate device and CMOS device is that the former has an additional floating gate which is created by two steps (Deposit Polysilicon (Floating gate), Dope Polysilicon (Floating gate) in the flow. These figures below illustrate the main process simulations using TCAD based on the design flow chart presented above (Figure 3a-3h).

The fabrication process starts from creating P-substrate (initial surface thickness = 1μm) with Boron at a concentration of 1.0e14 cm^{-3} (Figure 3a). Next, a mesh is defined, and the density of the mesh is a trade-off between accuracy and simulation time. After the mesh and wafer definition, a 0.45μm thick Epitaxy layer with Arsenic at a concentration of 1.0e16 cm^{-3} is grown on the top to make device surface thickness increase to 1.45μm (Figure 3b). Then, a P well is implanted using Boron with a dose of 8e12 cm^{-3}. After that, the P well is also diffused with Nitro gas at 1200^{0}C for about 310 minutes (Figure 3c). Next, Locos and tunnel oxide layer are created (Figure 3d). Creating Locos is an important step in the fabrication of semiconductor devices for the purpose of isolating the operation of two devices on the same wafer, and Oxide is usually used for this isolation. The doping channel is created using Boron at 100KeV and a concentration of 2.5e12 cm^{-3} (Figure 3e). Figure 3f shows the device structure after Polysilicon (Floating gate) is deposited and doped. Figure 3g shows the device structure after Polysilicon (Control gate) is deposited and doped. The Floating gate, Control gate, Tunnel Oxide layer and Oxide-Nitride-Oxide layer which is between Floating gate and Control gate are etched. An oxide layer with a thickness of 0.1μm is deposited and etched on the top to protect the device by the next steps. The next step is to create Source and Drain gates with Arsenic at 50 KeV and a concentration of

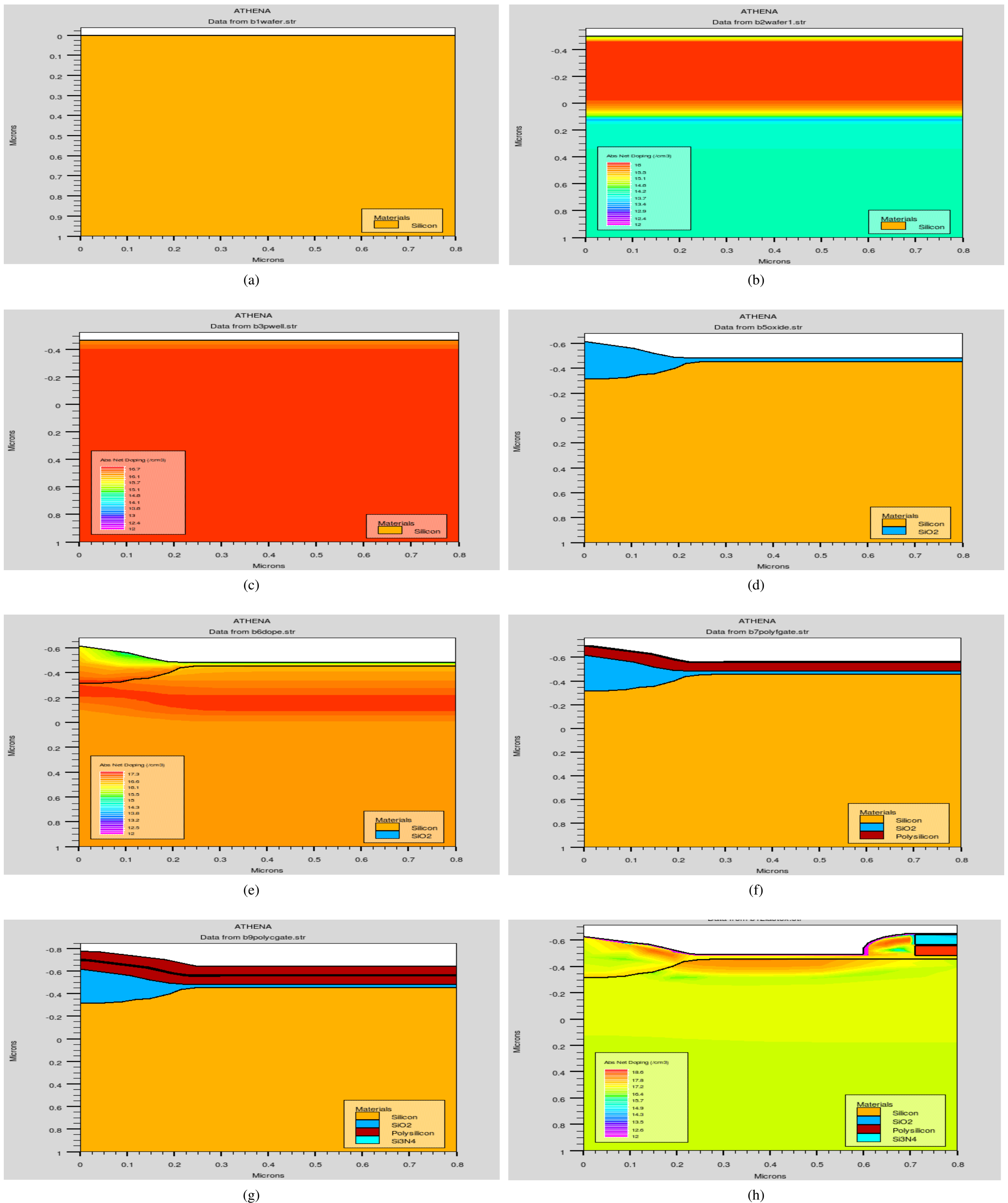

Figure 3: The main process simulations with TCAD including in a) Definition wafer b) Grow Epitaxial layer c) P well drive d) After creating Locos and grow Gate oxide e) Dope channel f) Create Floating gate and dope polysilicon g) Create Control gate and dope polysilicon h) After implant and diffuse S/D dopants

7e12 cm^{-3} (Figure 3h). After growing the protection layer, the final step is to deposit and etch Aluminum contacts for Source and Drain gates. The detailed process flow to fabricate the device is presented in Figure 2.

In this work, we propose to use the Athena tool to simulate the process of fabrication and the Atlas tool for operation simulations of the device. The following table gives the default parameter values in designing.

Table 1: Description And Default Parameter Values

DESCRIPTION	VALUE [μm]
Thickness of oxide-nitride-oxide nitride	0.013
Thickness of nitride spacer	0.002
Thickness of bottom oxide-nitride-oxide oxide	0.01
Thickness of top oxide-nitride-oxide oxide	0.001
Thickness of tunneling gate oxide	0.02
Thickness of control gate	0.075
Thickness of floating gate	0.075
Length of control gate	0.18
Length of floating gate	0.18

The complete 2D and 3D structures of the device in this work are given in Fig. 4 and Fig. 5, respectively. Regarding the 3D structure, the one is designed by using the 2D structure and the Devedit3D tool.

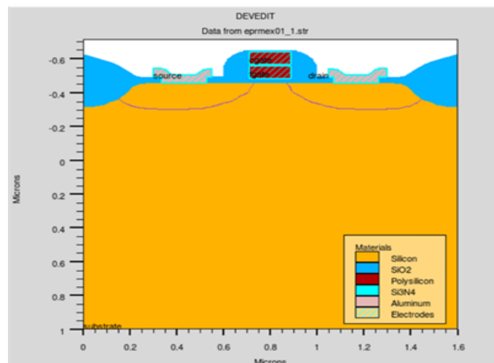

Figure 4: The 2D floating-gate device structure

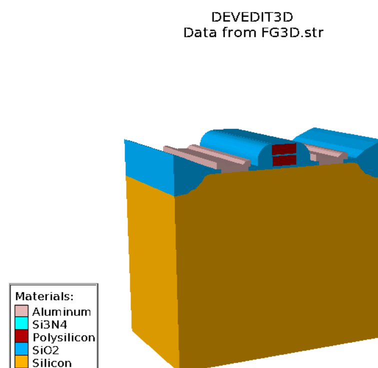

Figure 5: The 3D floating-gate device structure

4 Process Variation Results

This section presents the threshold voltage results of the floating-gate device designed in the previous section before programming and after programming.

Initially, before programming, there are no charges which are stored on the floating gate. The drain current – threshold voltage curve is shown in Fig. 6. The threshold voltage of the device is 0.6V.

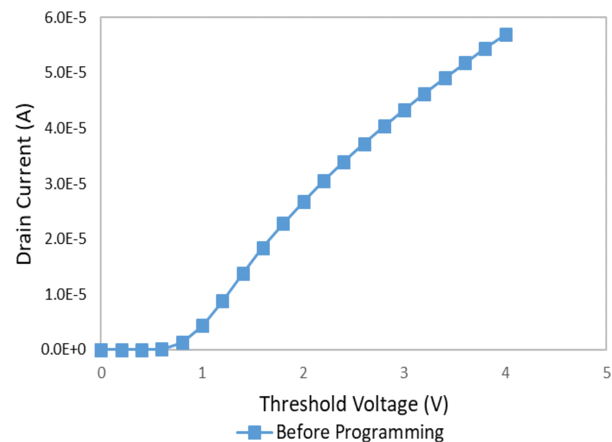

Figure 6: Threshold voltage of the device before programming process

After the programming process, the charges on the gate increase from 0C to around -3.5e-15C since the moving of electrons from the substrate. Meanwhile, the threshold voltage increases from 0.6V to approximately 6V. The charges on the gate and the threshold voltage in the programming process are given in Fig. 7 and Fig. 8, respectively. After that, the device is at the program state.

In contrast, as discussed in section II, the erasing process will remove all the negative charge on the floating gate which is generated from the programming process. Following this, the floating gate will have no charge, and the state of the device is as the initial (before programming state) or erasing state.

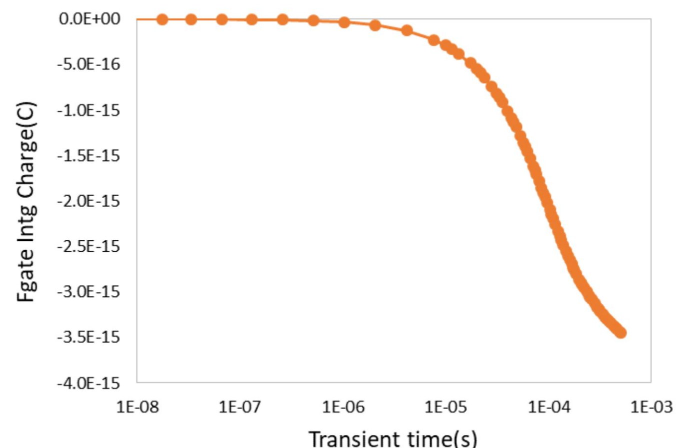

Figure 7: Floating gate charge in the programming process

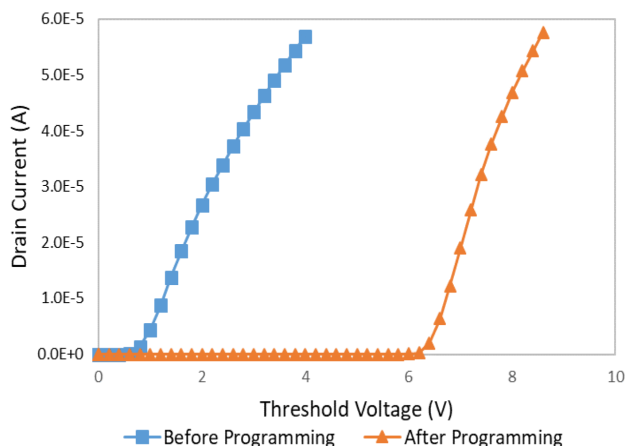

Figure 8: Threshold voltage of the device after programming process

The study of process variation demonstrates the effect of the threshold voltage on different geometrical parameters. In general, what stands out from the study is that whereas the threshold voltage is more sensitive to the gate length, tunneling gate oxide thickness, and bottom oxide-nitride-oxide oxide thickness, the threshold voltage is less sensitive to the gate width and nitride spacer thickness. The details of the study are given as follows.

4.1 Vary in values of the gate length

The figure in this section demonstrates the effect of the gate length parameter on the threshold voltage, it is clear that the increase in this parameter tends to a considerable increase in the threshold voltage, climbing around 18.33%, from 6V to approximately 7.1V. Thus, in the fabrication process, this parameter should be controlled carefully.

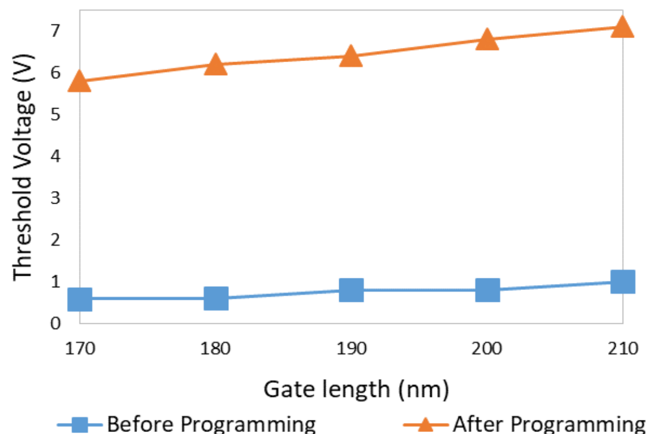

Figure 9: Gate length variation effects

4.2 Vary in values of the gate width

The figure below illustrates the change of the threshold voltage when the width parameter changes from 0.4μm to 1.6μm. This parameter is defined as a variable varied in the z-axis of the Devedit3D tool. In general, what stands out from the graph is that the voltage is not sensitive to this parameter. The threshold voltage remains stable at around 6V.

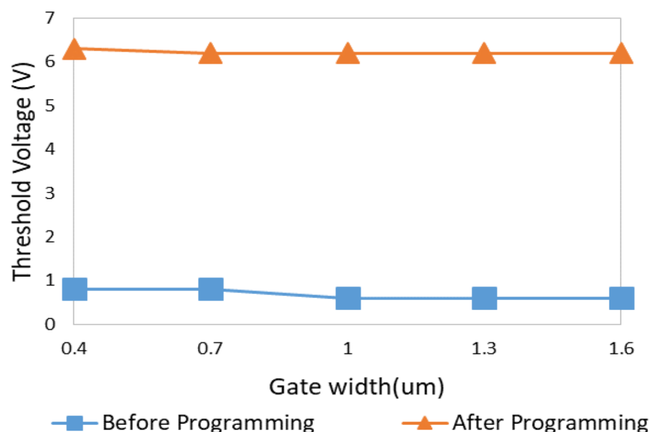

Figure 10: Gate width variation effects

4.3 Vary in values of the tunneling gate oxide thickness

The result is given in the graph in Fig. 11, it is clear that the change in tunneling gate oxide thickness results in a dramatic decrease in the threshold voltage when it varies from 20nm to 40nm. After programming, the voltage witnessed a drastic decrease, falling approximately 50% to about 3.2V. Hence, this is a very important parameter because the variation of the one causes a significant change in the operation of the device. With regard to the fabrication process, this parameter should be controlled carefully.

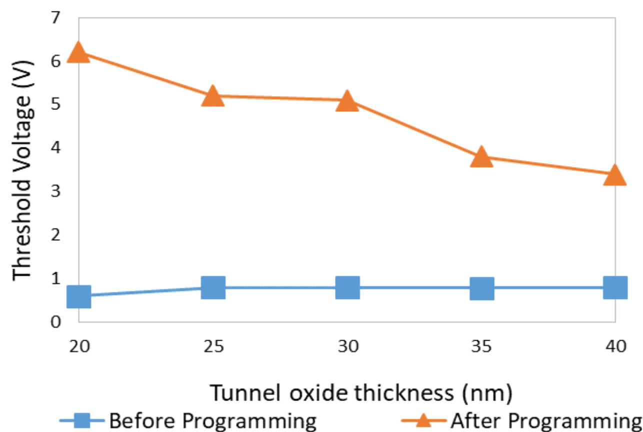

Figure 11: Tunneling gate oxide thickness variation effects

4.4 Vary in values of the bottom oxide-nitride-oxide oxide thickness

The graph in this section shows the results of the threshold voltage when the bottom oxide-nitride-oxide oxide thickness varied from 0.01μm to 0.03μm. Overall, it can be seen that the threshold voltage after programming experienced a considerable decrease of 23.33%, dropping from roughly 6V to approximately 4.6V. Thus, in the fabrication process, similar to the gate length and the tunneling gate

oxide thickness, this parameter should be observed carefully.

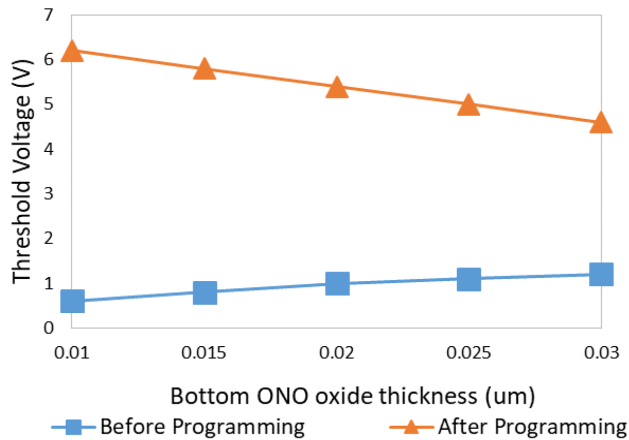

Figure 12: Bottom oxide-nitride-oxide oxide thickness variation effects

4.5 Vary in values of the nitride spacer thickness

The graph in the Fig. 13 presents the impact of the nitride spacer thickness parameter on the threshold voltage. It is clear that the impact of this parameter is very small. The threshold voltage after programming remaining between 5.9V and 6.1V throughout the study. Thus, the parameter would be controlled more easily than the others in the fabrication process.

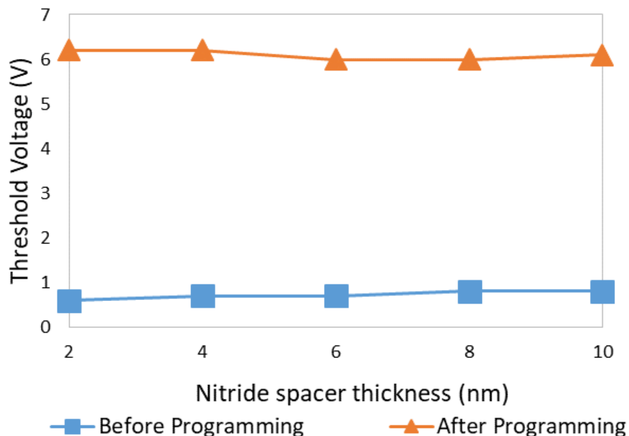

Figure 13: Nitride spacer thickness variation effects

5 Conclusion

This work is successful in the study of the process variation effects on the performance of a floating-gate device. The tunneling gate oxide thickness, bottom oxide-nitride-oxide oxide thickness, and gate length were found out to be sensitive to the threshold voltage, especially the tunneling gate oxide thickness parameter caused 50% change in threshold voltage. The others are 18.33% and 23.33%, respectively. While the gate width, nitride spacer thickness turned out to be less sensitive. This paper also successful in proposing a detailed flow and the parameter values to fabricate the complete floating-gate device based on CMOS 180nm process. The device which is designed by the flow worked as the expectation.

Conflict of Interest
The authors declare no conflict of interest.

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